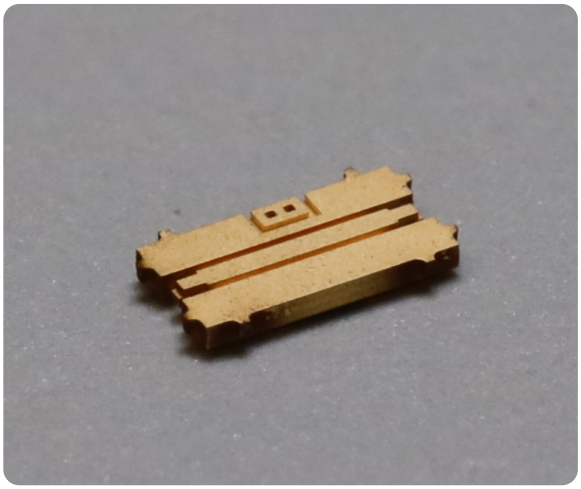
PSTLC02S Datasheet
Ultra-Broadband, Cross-Over Interconnect Bridge

General Description

The PSTLC02S is a 3.0 x 1.6 x 0.4 mm single-path cross-over, interconnect bridge. It has superior performance of typical 0.1dB IL and better than 20dB return loss over a frequency range of DC–67GHz. The isolation is >40dB over the frequency range. These devices were designed for high-density, multi-channel receivers to manage line routing while helping to minimize the number of PCB layers.



Applications

- EW
- Test and Measurement
- Satellite Communications
- Telecommunications
- RADAR

Benefits

- Small Size
- Wide operational range: DC–67GHz
- Low loss, high isolation
- CTE matched to PCB substrates

Features	
Frequency Range	DC–67 GHz
Insertion Loss	<0.2 dB
Channel Isolation	>40 dB
Package	3.0 x 1.6 x 0.4 mm, bottom-side SMT launches for reflow or epoxy attach

Performance Specifications

Table 1: RF Performance*

Parameter	Freq. Range (GHz)	Min.	Typ.	Max.	Unit
Insertion Loss	DC–67	–	0.1	0.2	dB
Return Loss	DC–50	20	25	–	dB
	50–67	15	20	–	dB
Channel Isolation	DC–50	40	45	–	dB
	50–67	35	45	–	dB

**Note: Min/Max performance based on operating temperature range.*

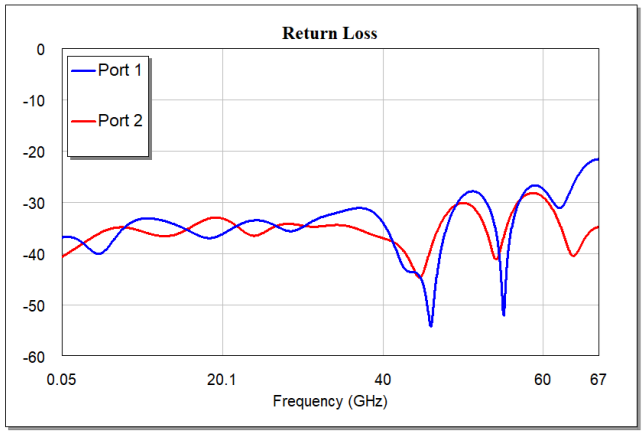
Table 2: Absolute Maximum Ratings

CW Power	10 W
Operating Temp.	-55°C to 125°C
Solder Reflow	260°C max. for 10 seconds, 3 cycles
Epoxy Attach	150°C max. for 90 minutes
Mechanical Vibration MIL-STD-883 M2026.4 (Cond. 1K)	45.0 Grms
Mechanical Shock MIL-STD-883 M2002.4 (Cond. B)	1500 G

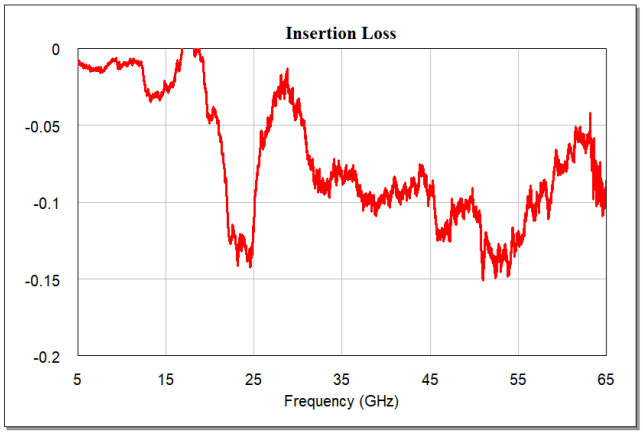
Typical Performance

Figure 1: RF performance

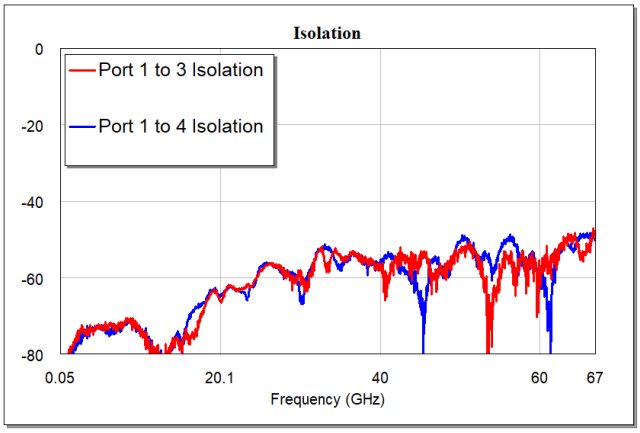
(a) Return Loss



(b) Insertion Loss



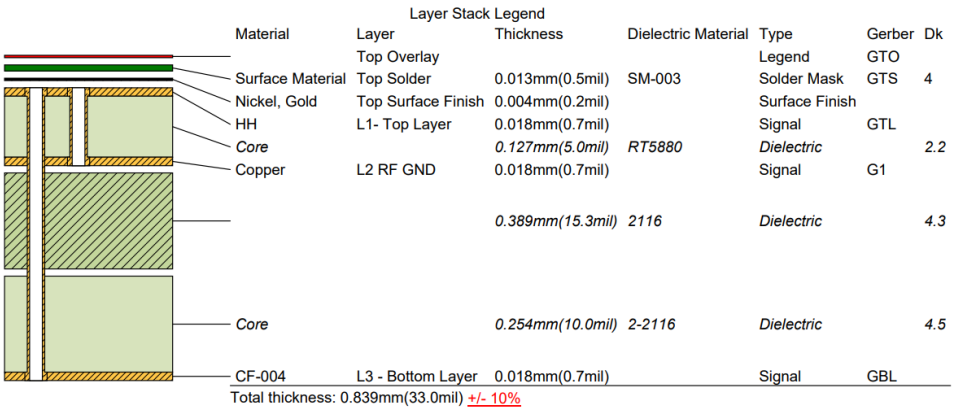
(c) Isolation



Plots above are measured, on PCB data.

PCB Guidelines

Figure 2: Recommended PCB Stackup



Layer Stack Legend

Material	Layer	Thickness	Dielectric Material	Type	Gerber	Dk
	Top Overlay			Legend	GTO	
Surface Material	Top Solder	0.013mm(0.5mil)	SM-003	Solder Mask	GTS	4
Nickel, Gold	Top Surface Finish	0.004mm(0.2mil)		Surface Finish		
HH	L1- Top Layer	0.018mm(0.7mil)		Signal	GTL	
Core		*0.127mm(5.0mil)*	*RT5880*	*Dielectric*		*2.2*
Copper	L2 RF GND	0.018mm(0.7mil)		Signal	G1	
		0.389mm(15.3mil)	*2116*	*Dielectric*		*4.3*
Core		*0.254mm(10.0mil)*	*2-2116*	*Dielectric*		*4.5*
CF-004	L3 - Bottom Layer	0.018mm(0.7mil)		Signal	GBL	

Total thickness: 0.839mm(33.0mil) +/- 10%

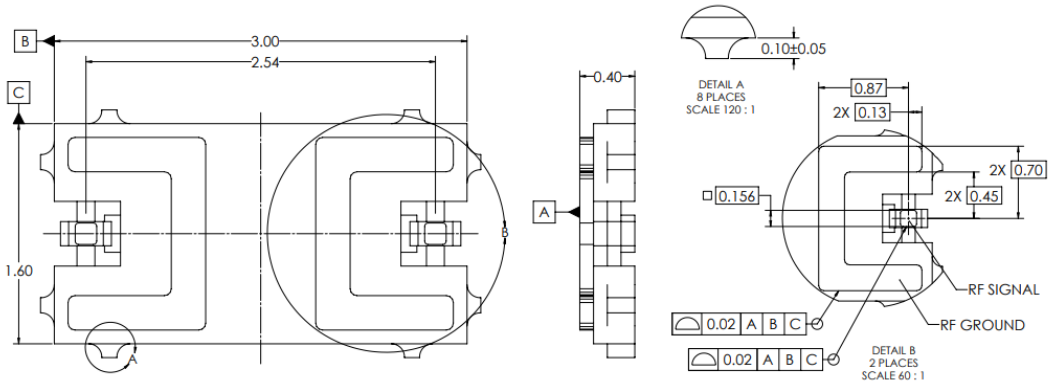
PCB Design Notes:

1. Use blind vias (Layer 1 to Layer 2 pair) around RF traces.
2. Use solid ground pour on all ground pins of the part to prevent parasitic inductances.
3. If deviating from the above stackup, the recommended PCB footprint may need to be adjusted for tuning purposes. Please contact Nuvotronics for assistance with tuning.
4. Follow stenciling guidelines outlined in IPC-7525C to prevent over-pasting RF launches (see ”PolyStrata SMT Assembly Guide” application note for details).

Mechanical Information

Figure 3: 2D Mechanical Drawing

Dimensions in mm



Note: Manufacturing tethers extend past the indicated dimensions of the part. See STEP model for details.

Additional Information

Table 3: Handling and Ordering Information

Storage	IAW IPC-4553A
ESD Sensitivity	None
Ordering Information	PSTLC02S
Standard Packaging	Gel Pack
Alternative Packaging	Tape & Reel
Component Termination Finish	Immersion Gold

Note: Detailed handling guidelines can be found in the "General Handling Guidelines" and "PolyStrata SMT Assembly Guide" application notes (see link below).

- Footprint DXF is available on request.
- Application notes on PCB integration are available at: https://www.nuvotronics.com/resources/