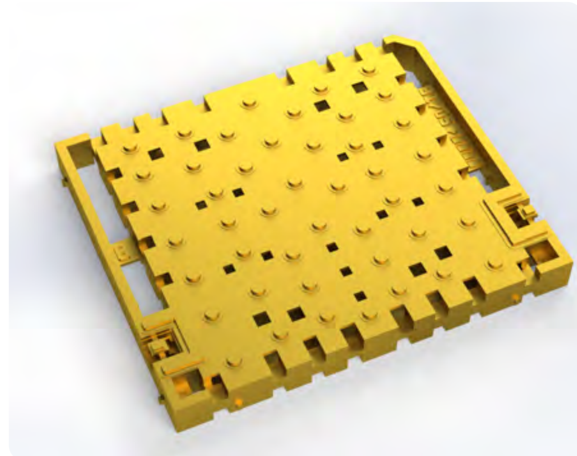
PSF1031705 Datasheet
SMT AQ408, 4th Order, 9.25 GHz Center Frequency Filter

General Description

The PSF1031705 is a 4th order interdigital filter, with a pass-band of 9.0–9.5 GHz. It provides <1.4dB insertion loss with high out of band rejection. The mounting interface provided is a SMT interface compatible with standard attach processes.



Applications

- General Purpose BPF

Benefits

- Low Loss
- High Rejection
- High Repeatability
- Compact Size
- CTE matched to PCB

Features	
Frequency Range	9.0–9.5 GHz, BPF
Insertion Loss	<1.4 dB across pass-band
Rejection	>40 dB out-of-band
Package	11.19 x 9.54 x 1.1 mm, bottom-side SMT launches for reflow or epoxy attach

Performance Specifications

Table 1: RF Performance

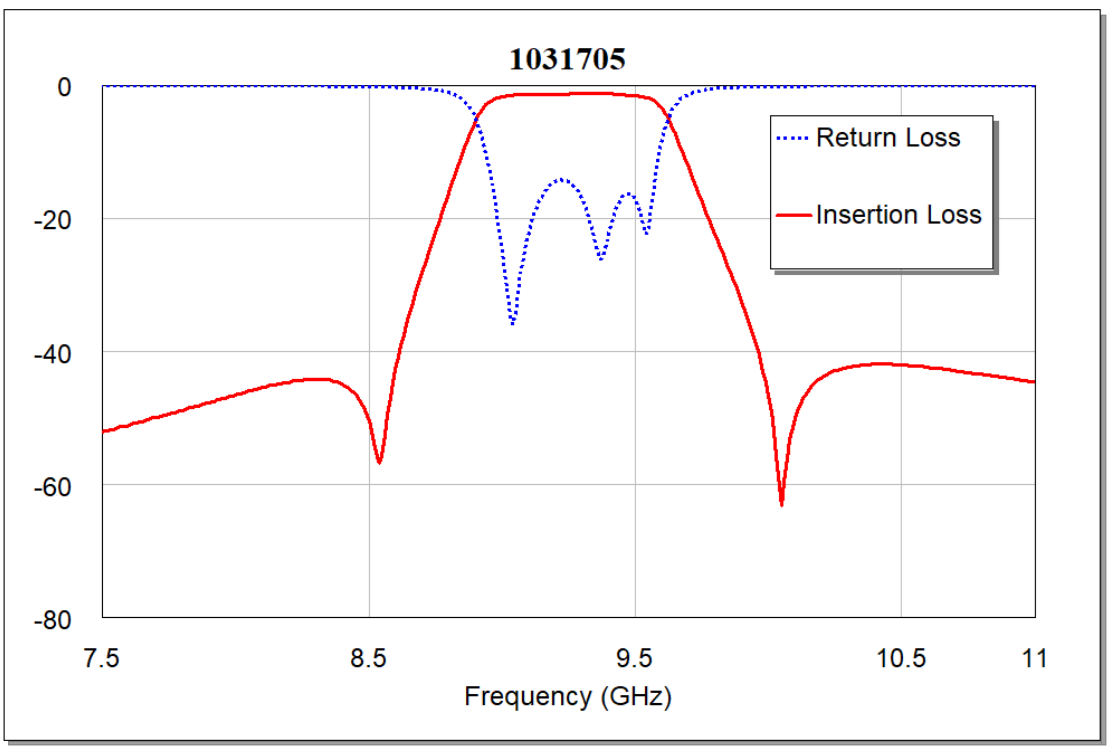
Parameter	Freq. Range (GHz)	Min.	Typ.	Max.	Unit
Return Loss	9.0–9.5	12	15	–	dB
Insertion Loss	9.0–9.5	–	1.1	1.4	dB
Lower Rejection	0–8.5	40	50	–	dB
Upper Rejection	10–18.0	40	50	–	dB

Table 2: Absolute Maximum Ratings

CW Power	5 W
Operating Temp.	-40°C to 85°C
Solder Reflow	260°C max. for 10 seconds, 3 cycles
Epoxy Attach	150°C max. for 90 minutes
Mechanical Vibration MIL-STD-883 M2026.4 (Cond. 1F)	20.0 Grms
Mechanical Shock MIL-STD-883 M2002.4 (Cond. A)	500 G

Typical Performance

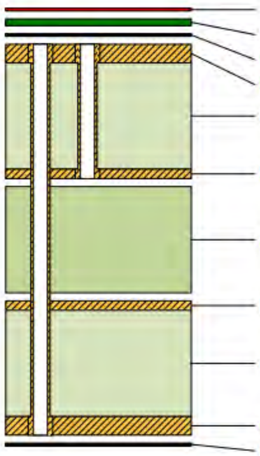
Figure 1: RF performance



Plots above are measured, on PCB data.

PCB Guidelines

Figure 2: Recommended PCB Stackup



Layer Stack Legend

Material	Layer	Thickness	Dielectric Material	Type	Gerber	Dk
	Top Overlay			Legend	GTO	
Surface Material	Top Solder	0.013mm(0.5mil)	SM-003	Solder Mask	GTS	4
Nickel, Gold	Top Surface Finish	0.004mm(0.2mil)		Surface Finish		
HH	L1- Top Layer	0.035mm(1.4mil)		Signal	GTL	
Core		*0.254mm(10.0mil)*	*RO4350B*	*Dielectric*		*3.66*
HH	L2 RF GND	0.018mm(0.7mil)		Signal	G1	
Prepreg		*0.381mm(15.0mil)*	*FR4*	*Dielectric*		*4.1*
HH	L3 - Inner 2	0.018mm(0.7mil)		Signal	G2	
Core		*0.254mm(10.0mil)*	*Core-028*	*Dielectric*		*4.3*
CF-004	L4 - Bottom Layer	0.035mm(1.4mil)		Signal	GBL	
Nickel, Gold	Bottom Surface Finish	0.004mm(0.2mil)		Surface Finish		

Total thickness: 1.015mm(40.0mil) +/- 10%

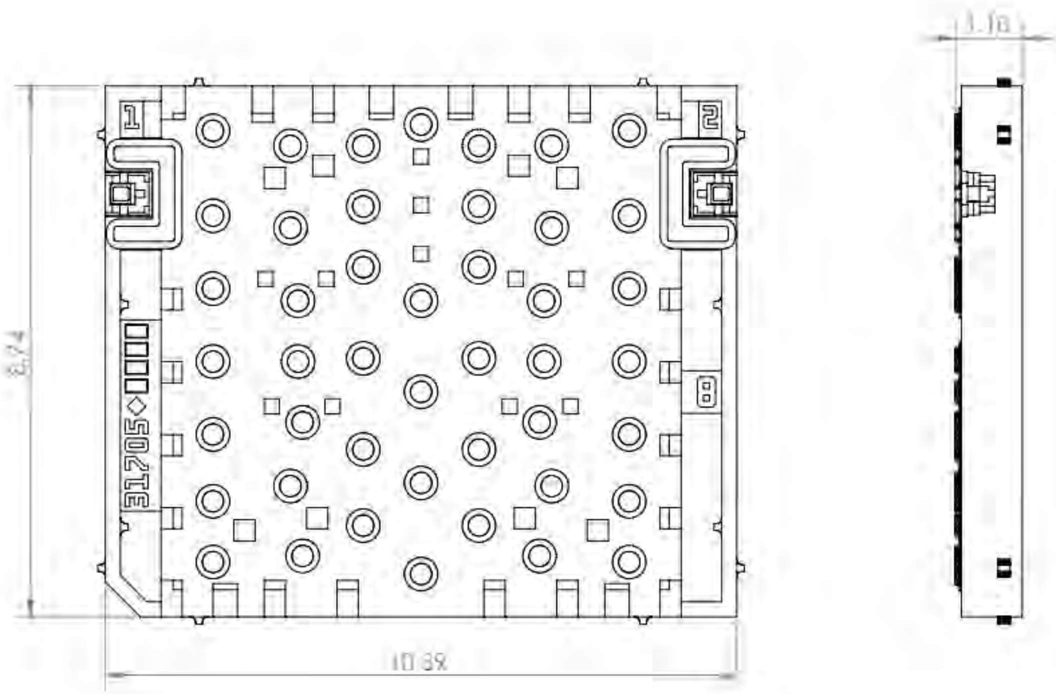
PCB Design Notes:

1. Use blind vias (Layer 1 to Layer 2 pair) around RF traces.
2. Use solid ground pour on all ground pins of the part to prevent parasitic inductances.
3. If deviating from the above stackup, the recommended PCB footprint may need to be adjusted for tuning purposes. Please contact Nuvotronics for assistance with tuning.
4. Follow stenciling guidelines outlined in IPC-7525C to prevent over-pasting RF launches (see "PolyStrata SMT Assembly Guide" application note for details).

Mechanical Information

Figure 3: 2D Mechanical Drawing

Dimensions in mm



Note: Manufacturing tethers extend past the indicated dimensions of the part. See STEP model for details.

Additional Information

Table 3: Handling and Ordering Information

Storage	IAW IPC-4553A
ESD Sensitivity	None
Ordering Information	PSF1031705
Standard Packaging	Gel Pack
Alternative Packaging	Tape & Reel
Component Termination Finish	Immersion Gold

Note: Detailed handling guidelines can be found in the "General Handling Guidelines" and "PolyStrata SMT Assembly Guide" application notes (see link below).

- Footprint DXF is available on request.
- Application notes on PCB integration are available at: https://www.nuvotronics.com/resources/