PolyStrata® PCB Integration Guide

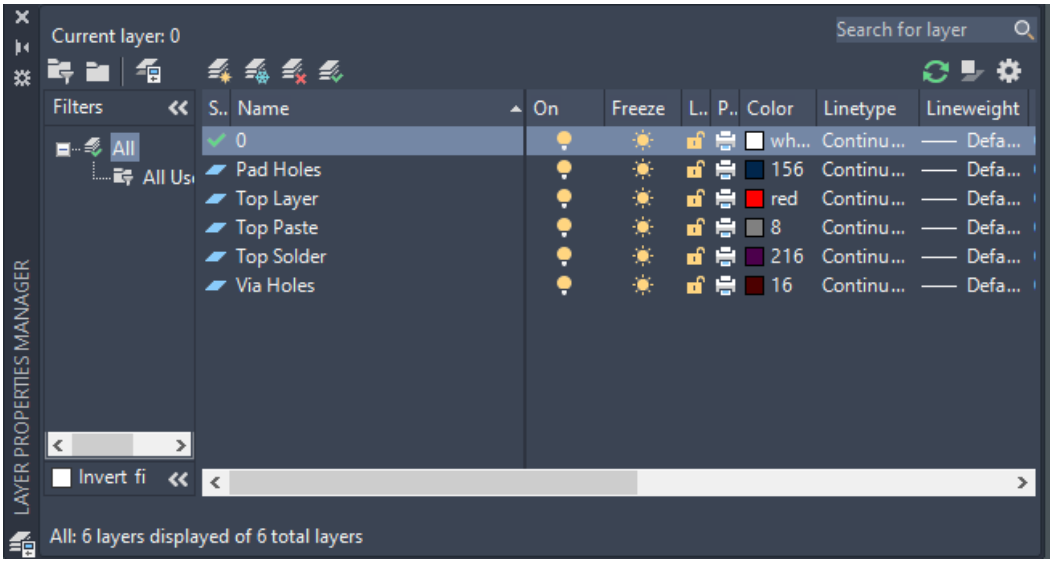
Purpose

This document is intended to outline general guidelines when integrating PolyStrata® surface mount components onto a PCB. This includes footprint creation/import, matching compensation for PolyStrata® to transmission line, setting up paste and solder resist layers, and design for manufacturability rules to include in a design.

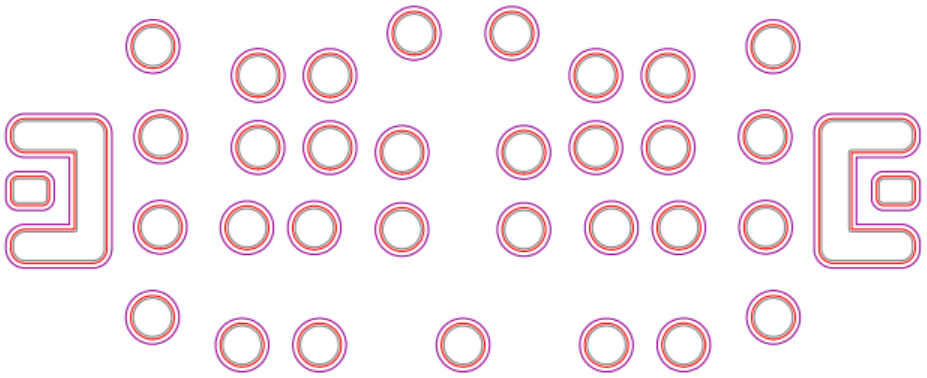
Footprint Import:

For all PolyStrata® SMT components, DXF drawings and native Altium libraries are available for importing into ECAD tools. Other formats may be available on request. Nuvotronics recommends importing the footprint using one of these provided formats for best results. Every ECAD tool will be slightly different with how DXFs are imported. However, the general procedure for importing DXFs is as follows:

1. Open the DXF in the preferred ECAD tool.
2. Assign layers from the DXF to the corresponding design layer:

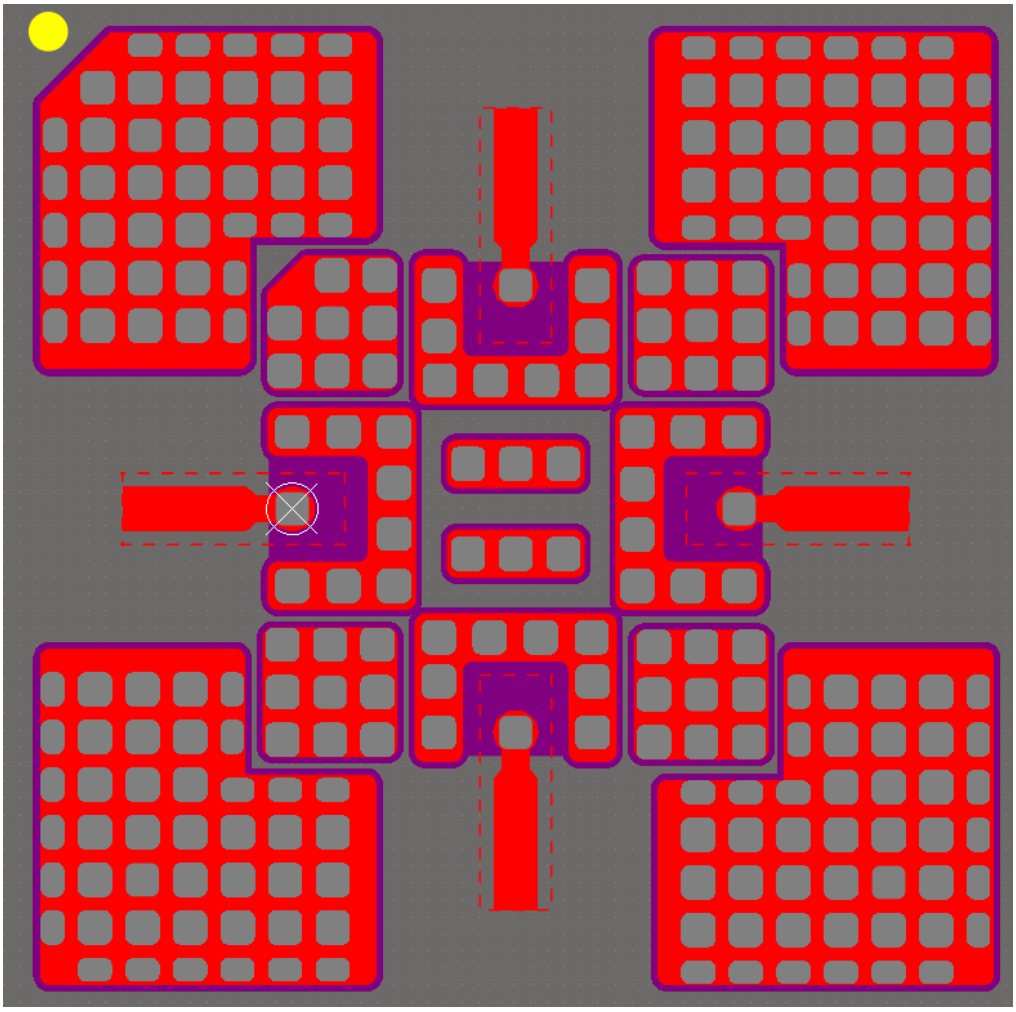


   a. Pad Holes: Only used on legacy parts for alignment pins to the PCB.
   b. Top Layer: Top copper and top keepouts. Filled copper will appear as solid polylines and keepouts will appear as dashed polylines.
   c. Top Paste: Recommended solder paste pattern.
   d. Top Solder: Top side solder-resist negative.
   e. Via Holes: Recommended via size/placement for isolation and matching.
3. After import, the footprint should be a collection of polylines:



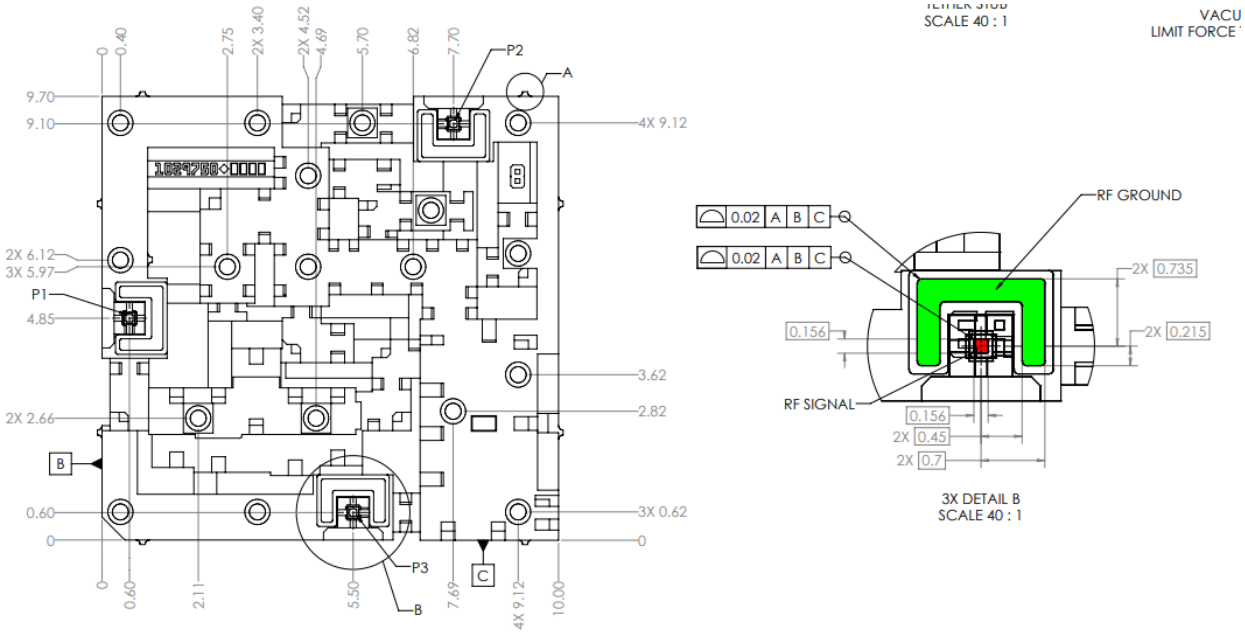
Each polyline represents the boundary edge of a fill. To finish the footprint, create a fill region inside each polyline boundary on the corresponding layers. For via placement, place the via in the center of the reference circles and set the annular ring size to the diameter of the reference.

4. The result of the import is shown below:



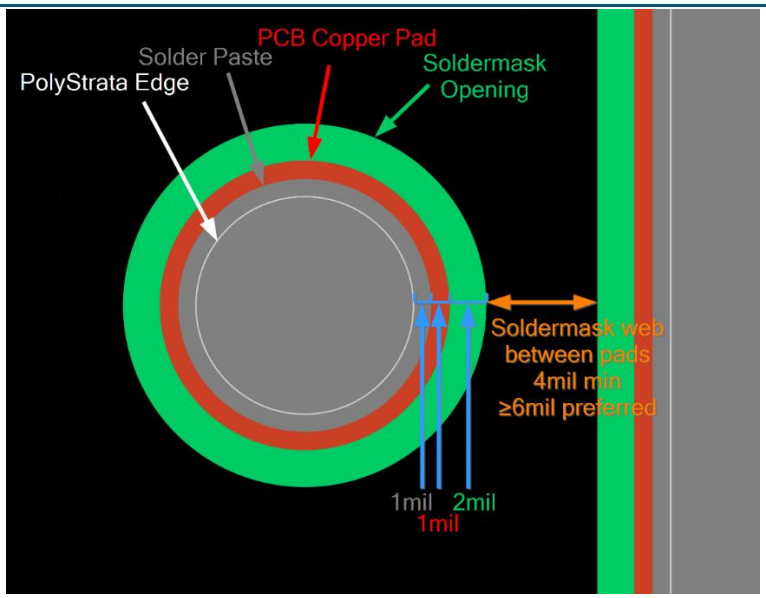
Footprint Creation:

Another approach to creating a footprint is using the Nuvotronics provided interface control drawing (ICD) with expansion design rules. An example of an ICD is provided below:

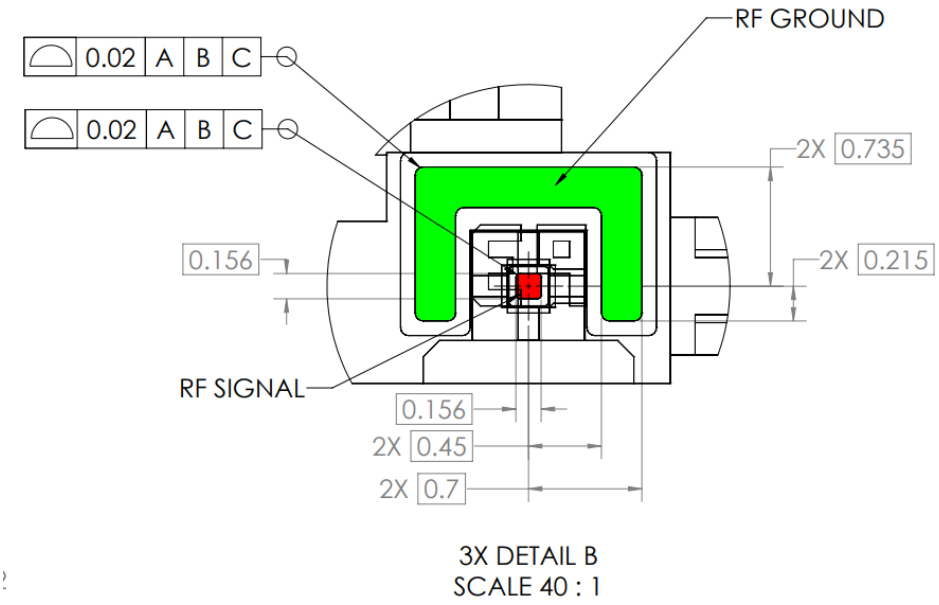


Ordinate dimensions of the PCB contact points are provided on the control drawing. Additionally, a breakout view of the SMT launch is provided to maintain the 50Ω reference plane at the contact point. The design procedure for creating the footprint is:

1. Create pads/landing points based on the provided PolyStrata® geometry.
2. Expand out the paste layer, copper layer, and solder resist by 1, 2, and 4 mil respectively:



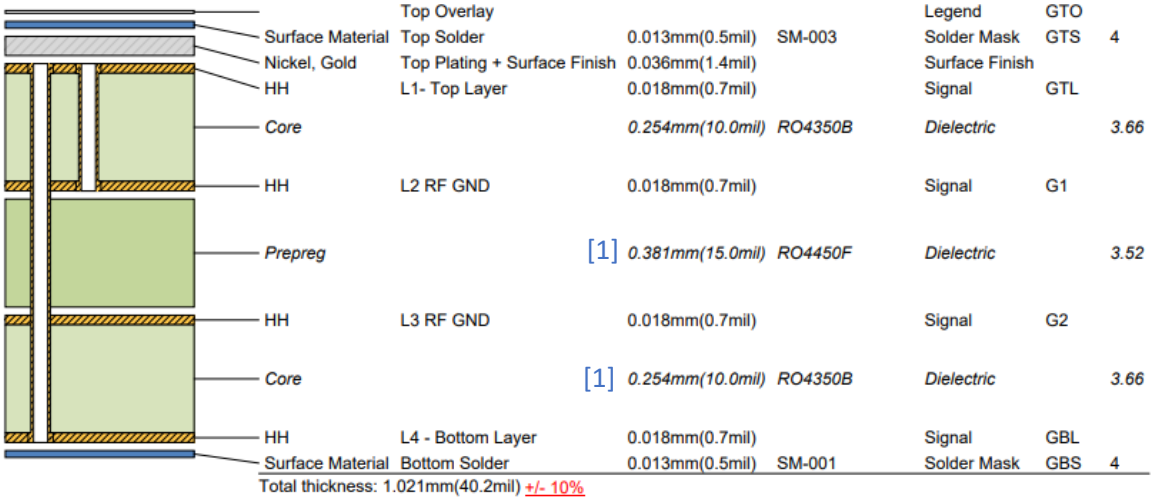
3. Add copper keepout around RF launch to match ground geometry:



There should be no copper fill between the center conductor and RF ground.

Re-tuning PolyStrata® to Co-planar Waveguide Transition:

The CPWG transition provided by Nuvotronics is tuned to the PCB stackup outlined in the part's corresponding datasheet. Several stackups may be used depending on the upper frequency range of the PolyStrata® part. Generally, the following 4-layer stackup using RO4350B dielectric is used unless otherwise noted:



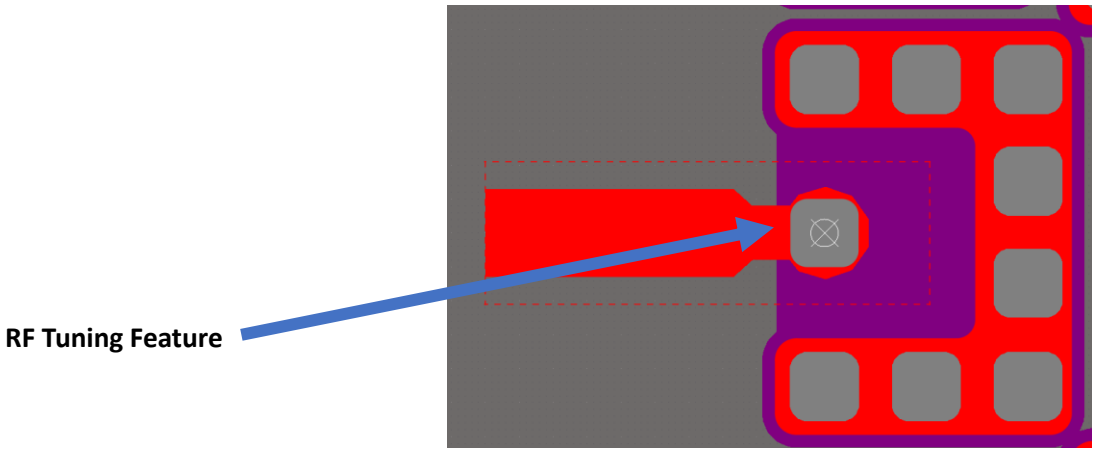
Layer Stack Legend

Material	Layer	Thickness	Dielectric Material	Type	Gerber	Dk
	Top Overlay			Legend	GTO	
Surface Material	Top Solder	0.013mm(0.5mil)	SM-003	Solder Mask	GTS	4
Nickel, Gold	Top Plating + Surface Finish	0.036mm(1.4mil)		Surface Finish		
HH	L1- Top Layer	0.018mm(0.7mil)		Signal	GTL	
Core		*0.254mm(10.0mil)*	*RO4350B*	*Dielectric*		*3.66*
HH	L2 RF GND	0.018mm(0.7mil)		Signal	G1	
Prepreg		[1] *0.381mm(15.0mil)*	*RO4450F*	*Dielectric*		*3.52*
HH	L3 RF GND	0.018mm(0.7mil)		Signal	G2	
Core		[1] *0.254mm(10.0mil)*	*RO4350B*	*Dielectric*		*3.66*
HH	L4 - Bottom Layer	0.018mm(0.7mil)		Signal	GBL	
Surface Material	Bottom Solder	0.013mm(0.5mil)	SM-001	Solder Mask	GBS	4

Total thickness: 1.021mm(40.2mil) +/- 10%

[1]: Note that these dielectrics may be FR4-2116 for PCBAs that only use CPWG and thus have no RF traces in layers 3-4.

For any deviations from this stackup, the tuning stub will need to be adjusted to accommodate for board parasitics in the transition. The PolyStrata® RF port is designed to be nominal 50Ω. The footprint land pattern will have a small series inductance to accommodate for the parasitic capacitance in the transition from rectangular coax on the PolyStrata® to CPWG on the board:



For more information or assistance on this tuning feature, please reach out to your Nuvotronics representative to connect with Applications Engineering.